

Serial No. 09/805,137  
Docket No. BUR919980050US3  
(BUR.006 DIV2)

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**AMENDMENTS TO THE CLAIMS:**

1-4. (Canceled).

5. (Previously presented) A method of updating a design of a semiconductor chip at a hardware description language (HDL) of simulation, to maximize an amount of logic that can be set to a previous cycle state, comprising:

automatically reading and setting a state value of control signals on a per-cycle basis in a template and updating the HDL design with new data;

changing a first predetermined value of the template to be set with the previous cycle state of the control signals; and

executing a test sweep to determine a "don't care" state of the control signals.

6. (Canceled).

7. (Original) The method according to claim 5, wherein said first predetermined value comprises a first non-zero value.

8. (Previously presented) The method according to claim 5, wherein said "don't care" state indicates a state at which a respective control signal of said control signals maintains a value from its previous cycle.

9-20. (Canceled).

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21. (Previously presented) A signal-bearing medium tangibly embodying a program of machine readable instructions executed by an apparatus to perform a method of updating a design of a semiconductor chip at a hardware description language (HDL) of simulation, to maximize an amount of logic that can be set to a previous cycle state, said method comprising:

automatically reading and setting a value of control signals on a per-cycle basis in a template and updating the HDL design with new data;

changing a first predetermined value of the template to be set with the previous cycle state of a control signal; and

executing a test sweep to determine a "don't care" state of the control signals.

22. (Canceled).